1 Introduction

The aXiom AX54A-0D is a Capacitive Touch and Force-sensing controller with the very highest performance, for use in demanding applications across markets such as Automotive, Industrial, White Goods and Medical.

The AX54A-0D is part of the TactoSense family of controllers that are optimised for button type interfaces. The high performance acquisition engine enables the controller to measure up to 26 Capacitive Touch Sensors (CTS) and 26 Capacitive Displacement/Force Sensors (CDS) concurrently. The designer is free to choose whether to use one or more of the device's sensing / control features from; Proximity Sensing, Touch Sensing, Force Sensing and Haptic/LED feedback. Any combination of these can be used concurrently. For example, the designer can create an array of touch buttons that also require force to activate them, or can create an array of force-only buttons behind a metal front panel. Each button can be individually configured to select its characteristics. Buttons can also be gated against one-another to allow features like guard channels, one-hot groups etc. Feedback can be autonomously triggered on various button events and is configurable as macro-driven I2C/GPIO or SPI sequences to be sent to external devices such as Haptics or LED controllers.

DISCLAIMER: This feature is under active development and is available upon request in engineering firmware builds only.

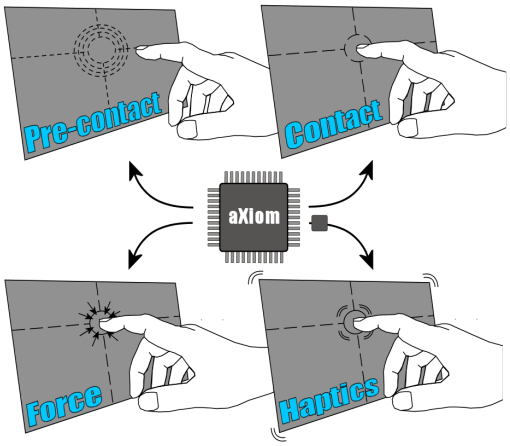


Figure 1-1: TactoSense Sensing and Control Capabilities

A Windows™ based software package, TouchHub2, is provided with the AX54A-0D to ease design and tuning tasks. This allows the designer to input simplified design choices and enables TouchHub2 to automatically create optimized tuning configurations.

[1]Subject to configuration.
[2]Pending

Features at a Glance

Capacitive Touch Controller

- Ultra high SNR: >80dB.
- Supports up to 26 touch sensing channels.
- Touch sensing through very thick plastic lenses and/or air gaps.
- Supports proximity sensing.
- Supports guard channel gating.
- Supports touch channel grouping and one-hot operation.
- All touches reported at a frame rate of up to 250Hz[1].
- Gloved touch operation.
- Water suppression and wet finger operation.
- Low emissions, low drive amplitude, high immunity to conducted interference.
- Host connection using SPI or I^2C slave with interrupt or LIN.
- 3V3 and 1V8 supply, no high voltage generators needed.
- Independent I/O voltage supporting 1.8V to 3.3V host signaling.
- Optional external synchronization e.g. induction hobs.

Force Controller

- Ultra high SNR: >80dB.
- Supports up to 26 force sensing channels.
- Displacements measured using patented capacitive transducers.
- Can detect displacement of cover panel <10um.
- Support for force sensing behind metal panels.
- No per-unit force calibration needed at production line.
- Highly tolerant of assembly variances.
- Two channel thermistor measurement for force temperature compensation.
- Two channel reference capacitor measurement for factory go-no-go testing.
- Sampling rate up to 250Hz[1].

Haptic Trigger

- User definable prox/touch/force feedback events.
- Trigger via master I2C to 3rd party driver chip.

General

- Low-cost construction, one chip solution for touch / force buttons with haptics.
- Register based tuning with non-volatile configuration storage.
- Field upgradable firmware.
- Sophisticated Built-In-Self-Test routines and diagnostics.
- Automotive AEC-Q100 grade 2 qualified[2].
- -40°C to +105°C ambient operating temperature.
- QFN88 package with side wettable flanks.

2 Ordering Information

Device	Package	Order Code	Shipping
AX54A-0D QFN88 Engineering Samples	QFN88 10x10x0.9x0.4 Side Wettable Flanks	Contact TouchNetix for availability	168 devices per tray
AX54A-0D QFN88 Industrial	QFN88 10x10x0.9x0.4 Side Wettable Flanks	Contact TouchNetix for availability	168 devices per tray
AX54A-0D QFN88 Automotive	QFN88 10x10x0.9x0.4 Side Wettable Flanks	Contact TouchNetix for availability	168 devices per tray

Contents

List of Figures

List of Tables

3 Device Pinout

3.1 Pin Map

3.1.1 QFN88

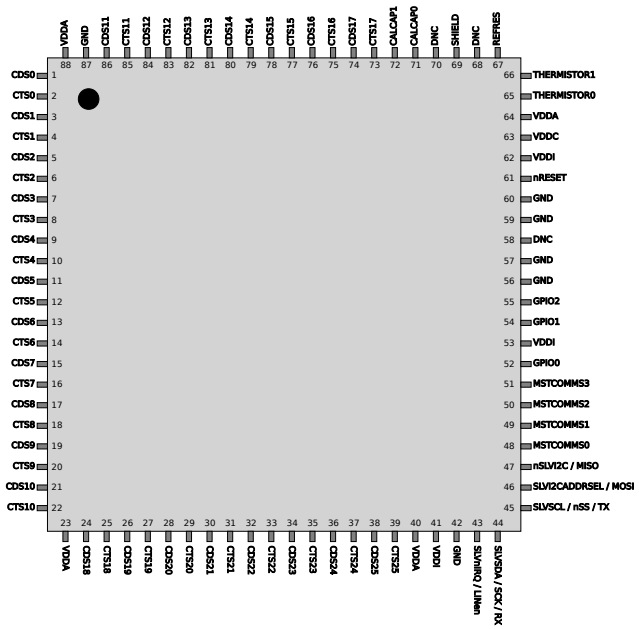


Figure 3.1.1-1: QFN88 Device Pinout (top view)

3.2 Pin Table

3.2.1 QFN88

Pin Number	Name	Class	Domain	Function	If not required	Notes
1	CDS0	AIO	VDDA	Sense pin	Leave no connect	For force sensing.
2	CTS0	AIO	VDDA	Sense pin	Leave no connect	For touch sensing.
3	CDS1	AIO	VDDA	Sense pin	Leave no connect	For force sensing.
4	CTS1	AIO	VDDA	Sense pin	Leave no connect	For touch sensing.
5	CDS2	AIO	VDDA	Sense pin	Leave no connect	For force sensing.
6	CTS2	AIO	VDDA	Sense pin	Leave no connect	For touch sensing.
7	CDS3	AIO	VDDA	Sense pin	Leave no connect	For force sensing.
8	CTS3	AIO	VDDA	Sense pin	Leave no connect	For touch sensing.
9	CDS4	AIO	VDDA	Sense pin	Leave no connect	For force sensing.
10	CTS4	AIO	VDDA	Sense pin	Leave no connect	For touch sensing.
11	CDS5	AIO	VDDA	Sense pin	Leave no connect	For force sensing.
12	CTS5	AIO	VDDA	Sense pin	Leave no connect	For touch sensing.
13	CDS6	AIO	VDDA	Sense pin	Leave no connect	For force sensing.
14	CTS6	AIO	VDDA	Sense pin	Leave no connect	For touch sensing.
15	CDS7	AIO	VDDA	Sense pin	Leave no connect	For force sensing.
16	CTS7	AIO	VDDA	Sense pin	Leave no connect	For touch sensing.
17	CDS8	AIO	VDDA	Sense pin	Leave no connect	For force sensing.
18	CTS8	AIO	VDDA	Sense pin	Leave no connect	For touch sensing.
19	CDS9	AIO	VDDA	Sense pin	Leave no connect	For force sensing.
20	CTS9	AIO	VDDA	Sense pin	Leave no connect	For touch sensing.
21	CDS10	AIO	VDDA	Sense pin	Leave no connect	For force sensing.
22	CTS10	AIO	VDDA	Sense pin	Leave no connect	For touch sensing.
23	VDDA	PWR		Analogue supply	Not applicable	
24	CDS18	AIO	VDDA	Sense pin	Leave no connect	For force sensing.
25	CTS18	AIO	VDDA	Sense pin	Leave no connect	For touch sensing.
26	CDS19	AIO	VDDA	Sense pin	Leave no connect	For force sensing.
27	CTS19	AIO	VDDA	Sense pin	Leave no connect	For touch sensing.
28	CDS20	AIO	VDDA	Sense pin	Leave no connect	For force sensing.
29	CTS20	AIO	VDDA	Sense pin	Leave no connect	For touch sensing.
30	CDS21	AIO	VDDA	Sense pin	Leave no connect	For force sensing.
31	CTS21	AIO	VDDA	Sense pin	Leave no connect	For touch sensing.
32	CDS22	AIO	VDDA	Sense pin	Leave no connect	For force sensing.
33	CTS22	AIO	VDDA	Sense pin	Leave no connect	For touch sensing.
34	CDS23	AIO	VDDA	Sense pin	Leave no connect	For force sensing.
35	CTS23	AIO	VDDA	Sense pin	Leave no connect	For touch sensing.
36	CDS24	AIO	VDDA	Sense pin	Leave no connect	For force sensing.
37	CTS24	AIO	VDDA	Sense pin	Leave no connect	For touch sensing.
38	CDS25	AIO	VDDA	Sense pin	Leave no connect	For force sensing.
39	CTS25	AIO	VDDA	Sense pin	Leave no connect	For touch sensing.
40	VDDA	PWR		Analogue supply	Not applicable	
41	VDDI	PWR		I/O supply	Not applicable	
42	GND	PWR		Supply and signal reference	Not applicable	
43	SLVnIRQ / LINen	OD / O	VDDI	Slave report ready interrupt OR LIN transceiver enable.	Leave no connect	Requires additional pull up if used Optionally serves as LIN transceiver enable output.
44	SLVSDA / SCK / RX	ODwpu / Iwpu	VDDI	Slave I^2C data OR SPI SCK OR LIN RX.	Not applicable	Requires additional pull up if using I^2C mode.
45	SLVSCL / nSS / TX	ODwpu / O (may change to Iwpu during startup).	VDDI	Slave I^2C clock OR SPI nSS OR LIN TX.	Not applicable	Requires additional pull up if using I^2C mode.
46	SLVI2CADDRSEL / MOSI	Iwpu	VDDI	Slave I^2C address select OR SPI MOSI.	Not applicable	In I^2C mode, controls address. In SPI mode becomes MOSI input from host.
47	nSLVI2C / MISO	Iwpu (may change to O during startup).	VDDI	Slave I^2C mode OR SPI MISO.	Not applicable	Sampled at reset; if low selects I^2C mode, if high selects SPI mode and becomes MISO output to host.
48	MSTCOMMS0	O / I / ODwpu	VDDI	Master Comms port	Leave no connect	
49	MSTCOMMS1	O / I / ODwpu	VDDI	Master Comms port	Leave no connect	
50	MSTCOMMS2	O / I / Odwpu	VDDI	Master Comms port	Leave no connect	
51	MSTCOMMS3	O / I	VDDI	Master Comms port	Leave no connect	
52	GPIO0	IOwpu	VDDI	General purpose I/O	Leave no connect	
53	VDDI	PWR		I/O supply	Not applicable	
54	GPIO1	IOwpu	VDDI	General purpose I/O	Leave no connect	Optionally serves as HSYNC input.
55	GPIO2	IOwpu	VDDI	General purpose I/O	Leave no connect	Optionally serves as VSYNC/EXTSYNC input.
56	GND	PWR		Supply and signal reference	Not applicable	
57	GND	PWR		Supply and signal reference	Not applicable	
58	DNC			Do not connect		
59	GND	PWR		Supply and signal reference	Not applicable	
60	GND	PWR		Supply and signal reference	Not applicable	
61	nRESET	Iwpu	VDDI	Hardware reset	Not applicable	May require additional bypass capacitor to GND for best EMC.
62	VDDI	PWR		I/O supply	Not applicable	
63	VDDC	PWR		Core supply		Output from internal LDO.
64	VDDA	PWR		Analogue supply	Not applicable	
65	THERMISTOR0	AIO	VDDA	Thermistor	Leave no connect	For force sensing temp compensation. 10K NTC.

Pin Number	Name	Class	Domain	Function	If not required	Notes
66	THERMISTOR1	AIO	VDDA	Thermistor	Leave no connect	For force sensing temp compensation. 10K NTC.
67	REFRES	AIO	VDDA	Reference resistor	Leave no connect	For thermistor calibration. 10K 1%.
68	DNC			Do not connect		
69	SHIELD	AO	VDDA	CTS and CDS shield pin	Not applicable	Shield driver for CTS and CDS sense pins.
70	DNC			Do not connect		
71	CDSCALCAP0	AIO	VDDA	Reference capacitor	Leave no connect	For force sensing factory test. 200pF 1%
72	CDSCALCAP1	AIO	VDDA	Reference capacitor	Leave no connect	For force sensing factory test. 100pF 1%
73	CDS17	AIO	VDDA	Sense pin	Leave no connect	For force sensing.
74	CTS17	AIO	VDDA	Sense pin	Leave no connect	For touch sensing.
75	CDS16	AIO	VDDA	Sense pin	Leave no connect	For force sensing.
76	CTS16	AIO	VDDA	Sense pin	Leave no connect	For touch sensing.
77	CDS15	AIO	VDDA	Sense pin	Leave no connect	For force sensing.
78	CTS15	AIO	VDDA	Sense pin	Leave no connect	For touch sensing.
79	CDS14	AIO	VDDA	Sense pin	Leave no connect	For force sensing.
80	CTS14	AIO	VDDA	Sense pin	Leave no connect	For touch sensing.
81	CDS13	AIO	VDDA	Sense pin	Leave no connect	For force sensing.
82	CTS13	AIO	VDDA	Sense pin	Leave no connect	For touch sensing.
83	CDS12	AIO	VDDA	Sense pin	Leave no connect	For force sensing.
84	CTS12	AIO	VDDA	Sense pin	Leave no connect	For touch sensing.
85	CDS11	AIO	VDDA	Sense pin	Leave no connect	For force sensing.
86	CTS11	AIO	VDDA	Sense pin	Leave no connect	For touch sensing.
87	GND	PWR		Supply and signal reference	Not applicable	
88	VDDA	PWR		Analogue supply	Not applicable	

Table 3.2.1-1: QFN88 Pin Table

Class	*Description*
PWR	Power pin
AI	Analogue input
AO	Analogue output
AIO	Analogue IO
I	CMOS input (no pull up)
Iwpu	CMOS input with weak pull up[3]
O	CMOS push-pull output
ODwpu	CMOS Open drain with weak pull up[3]
OD	CMOS Open drain no pull up
IO	CMOS input/output
IOwpu	CMOS input/output with weak pull up[3]

Table 3.2.1-2: Pin Classes

As a general convention, communication pin names are prefixed with "SLV" or "MST" to designate Slave or Master. Pin names with an "n" at the start of the function name designate an active-low signal e.g. MSTnIRQ is an active low interrupt from the Master. Also note that dual-mode pins are named (A) / (B), where (A) is the applicable name in the first mode and (B) in the second mode.

[3]Pull up/down intended as level keeper only.

4 Pin Descriptions

4.1 CDS0..CDS25

The CDS channels are used for force sensing. These channels connect to the zig-zag electrodes beneath the force sensor transducer VGE. The routing and layout of the connections to these pins is critical and is described in a separate application note. See **Appendix B References**.

4.2 CTS0..CTS25

The CTS channels are used for touch sensing. These channels connect to sense electrodes mounted behind a front panel. The routing and layout of the connections to these pins is critical and is described in a separate application note. See **Appendix B References**.

4.3 VDDA

The analogue sub-system's power supply connection, running at nominally 3.3V. Connect all VDDA pins to 3.3V. The VDDA supply must be low noise and well regulated. Each VDDA pin must have a parallel 22uF and 100nF ceramic capacitor within 2mm, bypassing to GND with a short low inductance PCB trace. An additional single bulk ceramic, tantalum or electrolytic capacitor of $\geq$ 22uF is required on the VDDA supply. Under most conditions its is acceptable to share this supply with VDDI[4].

These pins have special layout considerations. See **Appendix A.1.1 Layout and Routing Considerations for VDDA tracks** for further details.

4.4 VDDI

The I/O sub-system's power supply connection, running at nominally 1.8V to 3.3V. Connect all VDDI pins to this supply. The VDDI supply is used to define the interface logic level used to communicate with the host, so must be sufficiently well regulated to ensure reliable high speed comms. Each VDDI pin must have a 100nF ceramic capacitor within 2mm, bypassing to GND with a short low inductance PCB trace. If the VDDA and VDDI supplies are separate, an additional single bulk ceramic, tantalum or electrolytic capacitor of $\geq$ 1uF is required on the VDDI supply. Under most conditions it is OK to share this supply with VDDA, in which case route VDDI as a separate net and use a star point connection to VDDA to help to isolate noise on the two domains[4]. CMOS I/O pins should never exceed the limitations stated in Table 10.1-1 (Vpc and Vpa) during power up, operation or power down. See **Appendix A.1.1 Layout and Routing Considerations for VDDA tracks** for further details.

4.5 GND

The 0V power supply connection. Connect all GND pins to 0V.

4.6 SLVnIRQ / LINen

The device generates an interrupt whenever it has a report waiting to be read by the host. The slave interrupt pin asserts low in this case. It returns to a Hi-Z state when no reports are pending (but is weakly pulled up). The action of the host reading a report is to consume that report, and when all reports have been consumed the pin returns to Hi-Z (wpu). In order to affect an acceptably fast low-to-high transition in the presence of parasitic capacitance, an external pull up of 1K to 10K is required. The host device should use *level* triggering to sense the interrupt. Note the optional use as an enable for an external LIN transceiver when in LIN mode.

4.7 SLVSDA / SCK / RX

This pin serves different functions depending on the communication mode selected by the nSLVI2C pin:

Slave I²C Mode: The pin serves as the I²C Data pin to connect to the host. It has a weak internal

[4] Assuming the I/O level is 3.3V.

pull up which must be supplemented with a 1K to 10K pull up to achieve correct rise and fall times depending on capacitive loading.
Slave SPI Mode: This pin becomes the SPI SCK (clock) input from the host. In this mode no additional pull-up resistor is required.
Slave LIN Mode: This pin becomes the LIN RX input from a LIN transceiver. In this mode no additional pull-up resistor is required.

4.8 SLVSCL / nSS / TX

This pin serves different functions depending on the communication mode selected by the nSLVI2C pin:

Slave I²C Mode: This pin is the I²C Clock pin to connect to the host. It has a weak internal pull up which must be supplemented with a 1K to 10K pull up to achieve correct rise and fall times depending on capacitive loading.
Slave SPI Mode: This pin becomes the SPI active low Slave Select input from the host. In this mode no additional pull-up resistor is required.
Slave LIN Mode: This pin becomes the LIN TX output to a LIN transceiver. In this mode no additional pull-up resistor is required.

4.9 SLVI2CADDRSEL / MOSI

This pin serves different functions depending on the communication mode selected:

Refer to 7.2 for details of mode selections and how to connect this pin to an SPI interface.

4.10 nSLVI2C / MISO

This pin serves different functions depending on the communication mode selected:

Refer to 7.2 for details of mode selections and how to connect this pin to an SPI interface.

4.11 MSTCOMMS0

The device has a Master Communications port which can be controlled by a renderer in one of 3 modes: as a GPIO parallel output, as a master I²C interface or as a master SPI interface.
GPIO mode: this is the first output driver OUTA.
I²C mode: this is the Master I²C Data pin MSTSDA. It has a weak internal pull up which must be supplemented with a 1K to 10K pull up to achieve correct rise and fall times depending on capacitive loading.
SPI mode: this is the MOSI output data pin MSTMOSI to the slave.

4.12 MSTCOMMS1

The device has a Master Communications port which can be controlled by a renderer in one of 3 modes: as a GPIO parallel output, as a master I²C interface or as a master SPI interface.
GPIO mode: this is the second output driver OUTB.
I²C mode: this is the Master I²C Clock pin MSTSCL. It has a weak internal pull up which must be supplemented with a 1K to 10K pull up to achieve correct rise and fall times depending on capacitive loading.
SPI mode: this is the SCK clock output pin MSTSCK to the slave.

4.13 MSTCOMMS2

The device has a Master Communications port which can be controlled by a renderer in one of 3 modes: as a GPIO parallel output, as a master I²C interface or as a master SPI interface.
GPIO mode: this is the third output driver OUTC.
I²C mode: this is the active low interrupt pin MSTnIRQ. It has a weak internal pull up which may need to be supplemented depending on the nature of the driver connected to it. If the interrupt is shared between 2 or more devices then each must be capable of indicating via I²C commands whether it is

actively asserting its interrupt or not.
SPI mode: this is the MISO input data pin MSTMISO from the slave.

4.14 MSTCOMMS3

The device has a Master Communications port which can be controlled by a renderer in one of 3 modes: as a GPIO parallel output, as a master I²C interface or as a master SPI interface.
GPIO mode: this is the forth output driver OUTD.
I²C mode: not used.
SPI mode: this is the nSS active low slave select output pin MSTnSS to the slave.

4.15 GPIO0..GPIO2

General purpose I/O pins that can be configured and used by the host as required. Each one has an internal weak pull up included. Note the optional use of GPIO1 as an HSYNC input and GPIO2 as a VSYNC/EXTSYNC input (these optional selections are made via the device's configuration registers).

4.16 DNC

Do not connect. This pin has an internal connection to the device and must not be connected externally.

4.17 nRESET

This pin is the asynchronus master hardware reset. Asserted low it returns the device to its reset state. When high, the device operates as normal. The pin has a weak internal pull up which must be supplemented with a 1K to 5K pull up and optionally a 20 to 50nF ceramic bypass capacitor to GND[5] (to offer the best fast-transient immunity in harsh EMI applications).

4.18 VDDC

The core sub-system's power supply output, driven by an internal LDO running at nominally 1.8V. If there is more than one VDDC pin then connect them all together to form a single net. Each VDDC pin must have a parallel 22uF and 100nF ceramic capacitor within 2mm, bypassing to GND with a short low inductance PCB trace. No other connections to the VDDC net are permitted. See **Appendix A.1.1 Layout and Routing Considerations for VDDA tracks** for further details.

4.19 THERMISTOR0,1

The CDS measurements can be optionally temperature compensated using one or both thermistor readings. The thermistors are detailed in the Specifications section of this datasheet. For operation with a single thermistor, connect both pins together and connect to the single thermistor. When using two thermistors, the device will use the average reading to compensate CDS values (if enabled in the config). If temperature compensation is not required (disabled in config), leave both pins disconnected.

4.20 REFRES

The thermistor readings are calibrated against a reference resistor connected to this pin. The resistor is detailed in the Specifications section of this datasheet. If temperature compensation is not required (disabled in config), leave this pin disconnected.

4.21 SHIELD

The CTS and CDS sense pins must be routed using a shielding technique and a dummy electrode that is driven by this pin. This is described in a separate application note. See **Appendix B References**.

[5] Check the ability of the connected reset driver to support this capacitive load.

4.22 CDSCALCAP0,1

Each CDS channel is internally calibrated against a capacitor connected from its associated CALCAP pin to GND. The capacitors are detailed in the Specifications section of this datasheet.

5 Reference Schematic

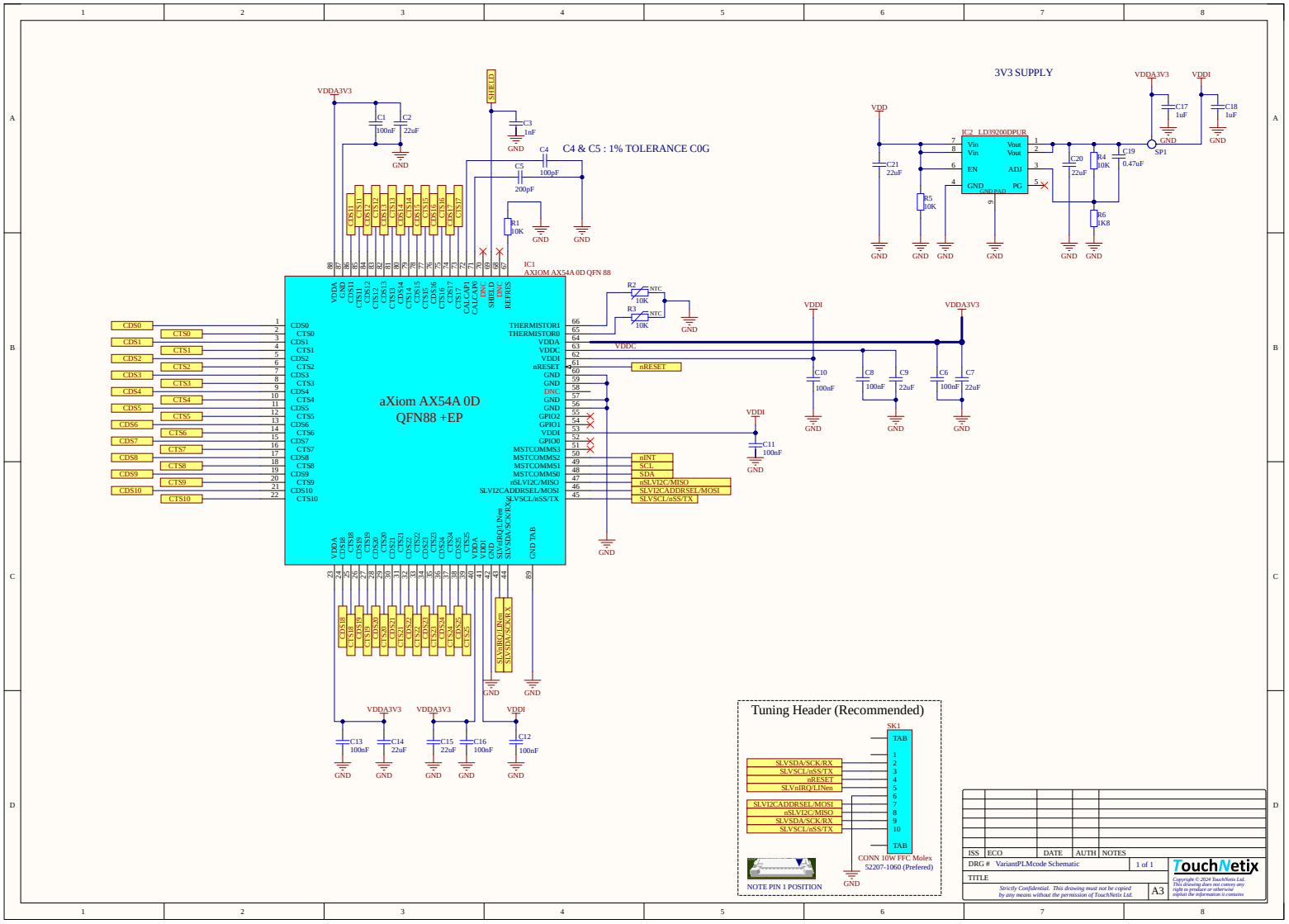


Figure 5-1: Reference Schematic (QFN88)

6 Sensing

6.1 Sensing Overview

The aXiom sensing architecture has been designed to measure capacitance, with a Signal-To-Noise ratio that goes far beyond existing solutions, whilst also being sympathetic to the diverse range of EMC and EMI challenges that are faced in real-world applications. Using a high purity narrow band drive waveform, with an amplitude of just 1.25V[6], the controller not only has extremely low Radiated Emissions, but is also sympathetic to the long term sensor aging problem, that is seen when operating at elevated temperature and humidity. This little-documented aspect of touch sensors, can only be addressed by using low amplitude DC-neutral drive techniques, to radically slow-down the effects of electro-corrosion, electro-migration and e-field induced damage to various metals and some polymeric materials. To pass stringent EMC tests, in particular those dealing with injected currents (Conducted Immunity), many competing controllers resort to high sensor drive amplitudes to improve their overall SNR. While this may be successful in one regard, it seriously compromises both sensor lifetime and Radiated Emissions. Coupled with drive waveforms that are often square in nature (leading to complex harmonic content), it can be seen that a pure low amplitude drive signal is a major advantage in tough environments. To measure capacitance using small signals in the presence of large amounts external noise, requires that the sensing architecture and the analogue front end of the device, is carefully optimized to be able to recover the carrier, even when this is hundreds of times smaller than the interference; techniques that are well understood in modern radio systems but that are seldom used in touch sensing.

The acquisition engine makes its measurements during a period called a Frame. Each frame is sub-divided into smaller time units called *Slots*. During a Frame different measurement tasks (Slots) are scheduled. Typically a Frame consists mainly of CTS and CDS Slots. There are also typically a small number of Slots used for housekeeping. To simplify things, TouchHub can automatically configure the Frame based on the system's requirements.

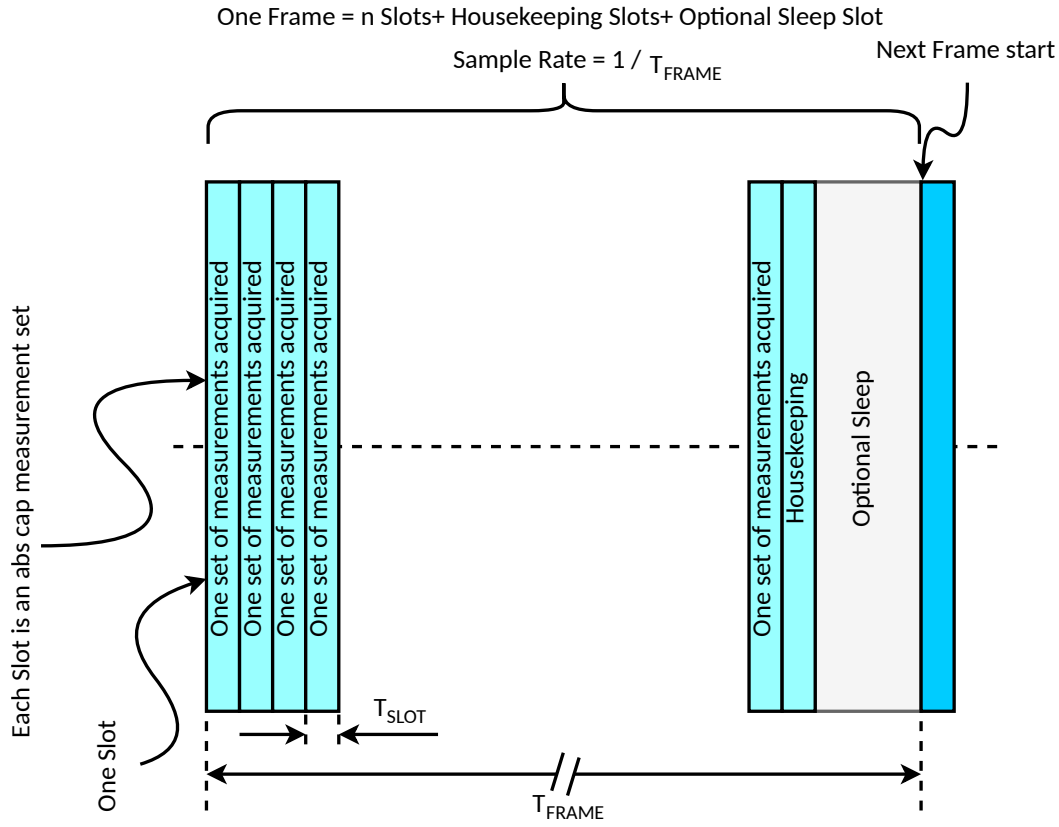


Figure 6.1-1: Acquisition Engine Frame Structure

[6] 2.5V pk-pk

The overall architecture of the AX54A-0D is shown below in simplified form.

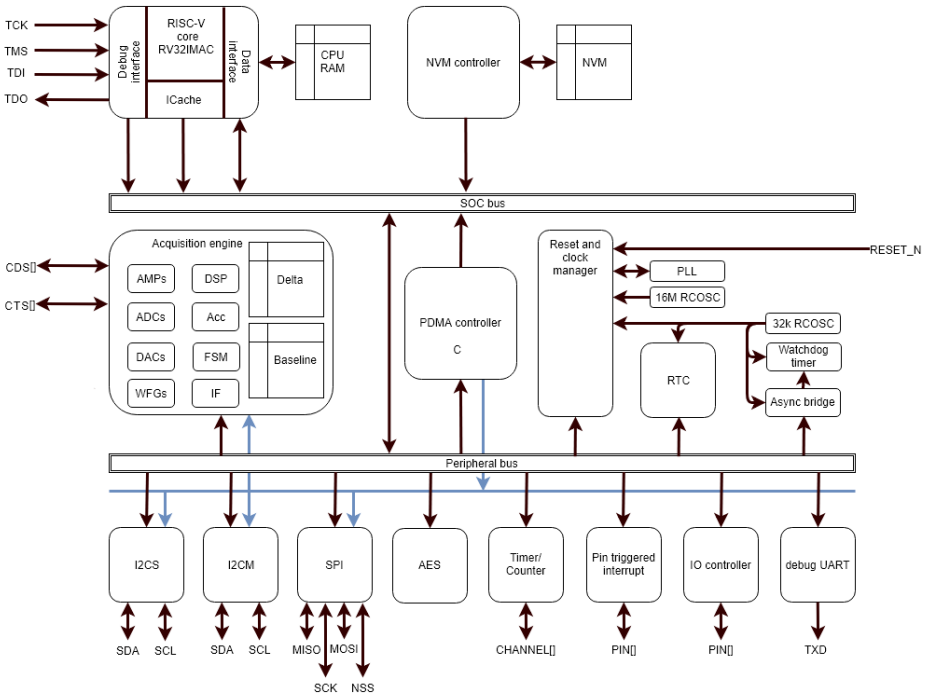


Figure 6.1-2: Simplified System Architecture

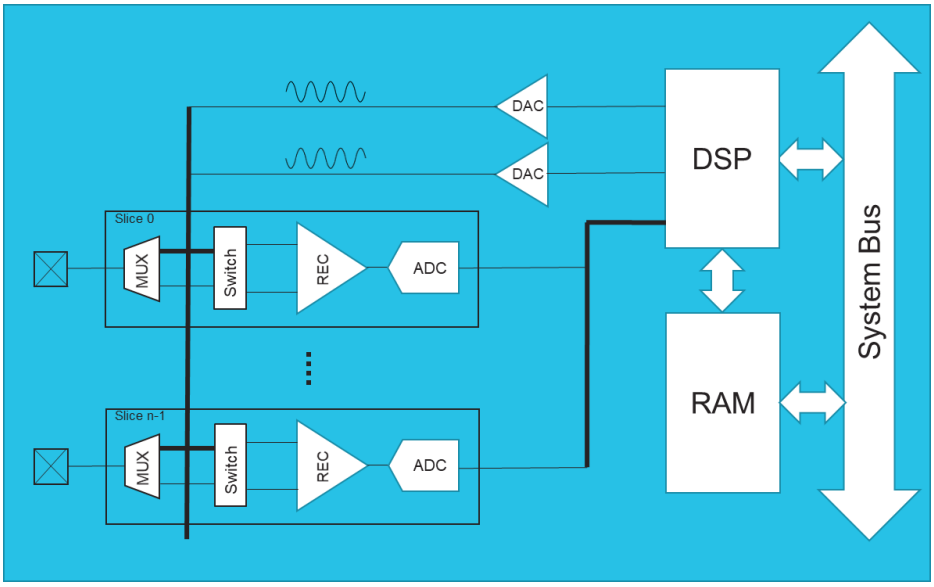


Figure 6.1-3: Simplified Sensing Architecture

6.2 Touch Sensing

The CTS channels of the AX54A-0D are all measured using an *absolute capacitive* measurement technique ("abs-cap") using common measurement engine settings, such as gain, frequency etc. Abs-cap will measure the total capacitance to ground of each of the channels, including any parasitic capacitance formed by PCB traces, nearby grounds etc. It is therefore desirable that the capacitive loading on the channels is equalized as far as is practical; the most heavily loaded channel will set the gain for all others and hence will be the limit for sensitivity. While each channel can be configured to set its own threshold, the underlying SNR will be dominated by the most heavily loaded channel. As a guide, try to keep the area of a touch electrode within +/-25% of the average area, and keep the electrode routing back to the controller surrounded by the SHIELD signal. It is best to group all CTS traces on the PCB and keep them separate to the CDS traces.

CTS channels can be connected to typical touch electrodes such as PCB pads or other conductive shapes. These can be mounted to a front panel using adhesive tapes or even simply pressed to the surface (so long as the mounting is stable and doesnt move or flex in use). For a system that will use Touch and Force, the CTS channels can be connected to the VGE whilst it is also acting as the force transducer on a CDS channel. In this way the VGE serves two roles

1. During CTS measurements its upper flat face acts as a touch sensing pad
2. During CDS measurements it serves as a DC reference potential to transduct movement-to-capacitance change in the zig-zag electrode beneath the curved surface of the VGE

In this case the VGE is simply pushed up against the inside of the sensing surface. More details of this type of TactoSense configuration can be found in **TNxAN00088 aXiom TactoSense Design Guide**.

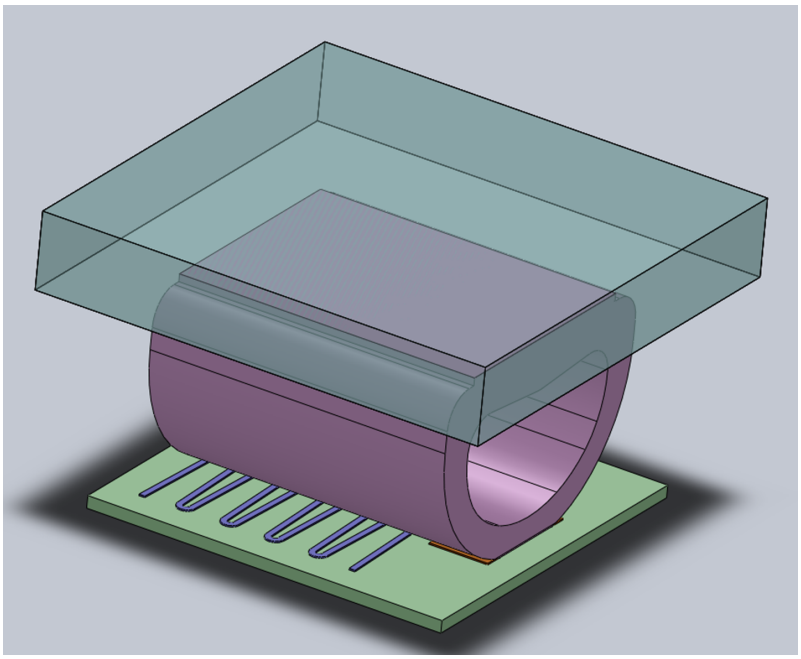


Figure 6.2-1: TactoSense Dual Mode Touch and Force

6.3 Force Sensing

The CDS channels of the AX54A-0D are all measured using an *absolute capacitive* measurement technique ("abs-cap") using common measurement engine settings, such as gain, frequency etc. Abs-cap will measure the total capacitance to ground of each of the channels, including any parastic capacitance formed by PCB traces, nearby grounds etc. It is therefore desirable that the capacitive loading on the channels is equalized as far as is practical; the most heavily loaded channel will set the gain for all others and hence will be the limit for sensitivity. While each channel can be configured to set its own threshold, the underlying SNR will be dominated by the most heavily loaded channel. As a guide, try to keep the area of a zig-zag electrode within +/-25% of the average area, and keep the electrode routing back to the controller surrounded by the SHIELD signal. It is best to group all CDS traces on the PCB and keep them separate to the CTS traces.

CDS channels must be connected to specific force sensing zig-zag style electrodes formed on a PCB or as part of a touch sensor. These electrodes are positioned under the curved surface of what is known as "VGE" which is used by the CDS channels to act as the force transducer. Small displacements transmitted from a front panel, which compress the VGE slightly onto the zig-zags, create a change in absolute capacitance of the zig-zag. It is possible to also use the VGE as the touch sensor in a dual mode design. More details of this type of TactoSense configuration can be found in **TNxAN00088 aXiom TactoSense Design Guide**.

6.4 EMC Features

One of the toughest challenges faced by capacitive touch sensors, is that of achieving high electrical noise immunity to conducted interference. The reason is simple: in most typical electronic systems we only need to worry about noise on the power supplies relative to our own GND (0V), which is local to the system. Excess noise can always be filtered out. In a capacitive touch system, part of the sensing current travels via a capacitively coupled route, through the touching finger and back to the controller *via a 3rd terminal; earth*. So noise that is *common* to power *and* GND relative to earth, will appear in the capacitive measurement when, and only when, a touch is applied. In some compliance tests, this immunity aspect is checked by injecting a *common mode* signal and sweeping it from 150KHz to 80MHz, 80% amplitude modulated. This causes a voltage disturbance of nearly 50V peak-to-peak with respect to earth[7]! Noise of this type is encountered in many industrial, medical and automotive environments, caused by switch mode power supplies, inductive coupling between equipment cables etc. Clearly, because the noise is "earth referred" there is no obvious conventional way to filter it.

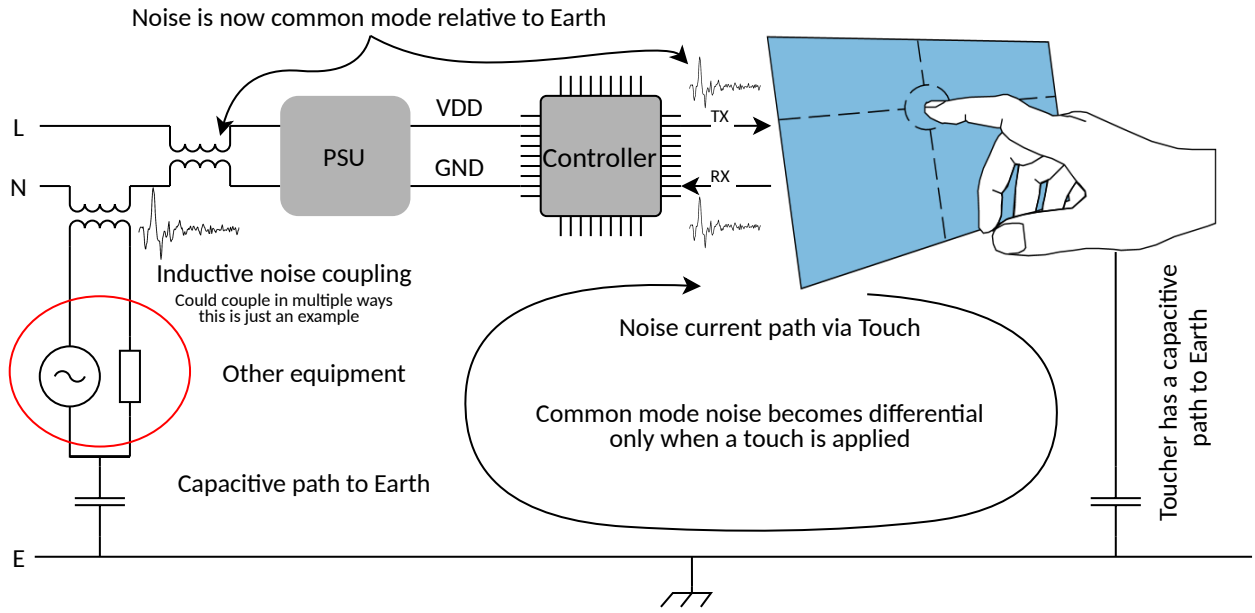


Figure 6.4-1: Example Common Mode Noise From "Other" Equipment

The nature[8] of a typical touch sensor is that capacitance measurements at a frequency between 50 and 500KHz tend to be optimal. Clearly this frequency range overlaps the test band mentioned above; injecting noise at or near the measurement frequency will directly affect the measurement. In order to counter this, the AX54A-0D is frequency agile, being able to move its measurement frequency at will. This is known as *frequency hopping* and is a well understood method for avoiding interference in many aspects of electronics and radio communications[9]. The AX54A-0D uses a very narrow bandwidth to measure capacitance. This has the great advantage that in a congested spectrum with narrow *quiet gaps*, it is still possible to re-locate the acquisition frequency to affect low noise measurements. Many competing touch devices use an *integration* technique, employing an integrator with a sampled input. This gives rise to an extremely wide and complex *reception spectrum*[10], making it hard to hop away from interference. A second advantage that narrow band demodulation offers, is that it is possible to very accurately measure the amount of external noise present at any moment; the AX54A-0D does this continuously each frame and hence it can react instantly if noise suddenly appears in the system. Competing systems can sometimes be fooled into thinking that there is zero noise, when certain noise frequencies are injected, and hence their measurements fail when no preventative steps are taken to frequency hop. The AX54A-0D can never be fooled in this way. The AX54A-0D also sets new standards in its ability to maintain several internal operating points, allowing it to hop quickly and seamlessly between frequencies.

[7] e.g. EN61000-4-6 Testing and measurement techniques - Immunity to conducted disturbances, induced by radio-frequency fields: Level 3.

[8] i.e. its -3dB frequency response.

[9] Invented c. 1942 for guided torpedo anti-jamming.

[10] the sampling window imposes a $\frac{sin(x)}{x}$ frequency response characteristic which is full of slowly reducing lobes and few, very narrow gaps to hop to.

To further protect the AX54A-0D against EMI, the signal path in the analogue front end, uses techniques to avoid its amplifiers from over-ranging in the presence of very high levels of interference. Even when such counter measures are employed, the touch report stability is still industry leading, thanks to the high SNR of the acquisition engine.

So far we have talked only about immunity to interference, but in some applications, emissions are just as big an issue. The AX54A-0D drives the sensor with a pure 1.25V amplitude sinusoidal waveform at a single frequency. Compare this to many competing devices that drive the sensor using a square wave at up to 30V peak-to-peak, leading to problems when trying to pass emissions certification.

As previously mentioned, the proprietary CDS transducer electrode arrangement used with aXiom force sensing, has the great advantage that it tends to form a GND sandwich and hence is strongly self shielding, simplifying both conducted and radiated EMC aspects.

7 Host Interfaces

7.1 Available Interfaces

The AX54A-0D offers three ways to communicate with the host;

1. A slave I²C interface consisting of the following pins (taking the name **before** the first "/"): (**SLVSDA / SCK / RX**), (**SLVSCL / nSS / TX**) and an interrupt (**SLVnIRQ / LINen**). Rates up to 400KHz are supported.
2. A slave SPI interface consisting of the following pins (taking the name **after** the first "/"): (**SLVI2CADDRSEL / MOSI**), (**nSLVI2C / MISO**), (**SLVSDA / SCK / RX**), (**SLVSCL / nSS / TX**) and an interrupt (**SLVnIRQ / LINen**). Rates up to 4MHz are supported.
3. A LIN slave UART interface consisting of the following pins (taking the name **after** the second "/"): (**SLVSDA / SCK / RX**), (**SLVSCL / nSS / TX**) and an optional use of (**SLVnIRQ / LINen**) (taking the name **after** the "/") to control an external transceiver's enable input. Rates up to 20KBaud are supported.

7.2 Mode Selection

Two pins control which host interface is selected: **nSLVI2C / MISO** and **SLVI2CADDRSEL / MOSI** . The two pins are sampled as the device starts up (from a power on, or reset event). Note that the **nSLVI2C / MISO** pin includes a weak pull-up that must be overridden either by tying it to GND (for I²C mode) or by **pulling up** with a supplemental resistor to VDDI (for SPI mode)[11] (see **4.10 nSLVI2C / MISO**).

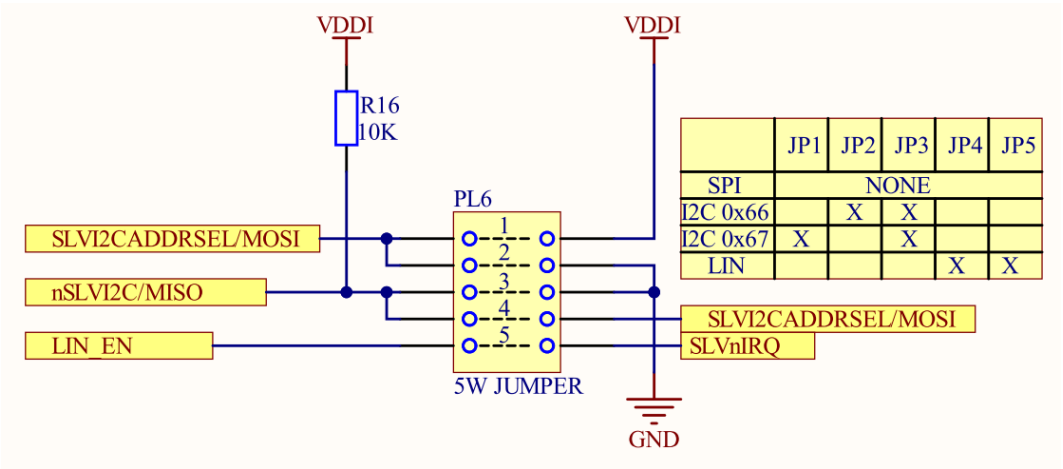


Figure 7.2-1: Communication Mode Selection

[11] In SPI mode the pin changes to become an output and hence must **not** be pulled up by tying directly to VDDI.

7.3 Slave I²C Mode

7.3.1 Slave Address Selection

Two different Slave I²C addresses can be selected with the **SLVI2CADDRSEL / MOSI** pin. The pin is sampled as the device starts up (from a power-on, or reset event):

SLVI2CADDRSEL / MOSI level	Slave I²C Address (7-bit hex)
low	0x66
high	0x67

Table 7.3.1-1: Slave I²C Address Selection

See **4.9 SLVI2CADDRSEL / MOSI** for notes on terminating this pin.

7.3.2 Connections

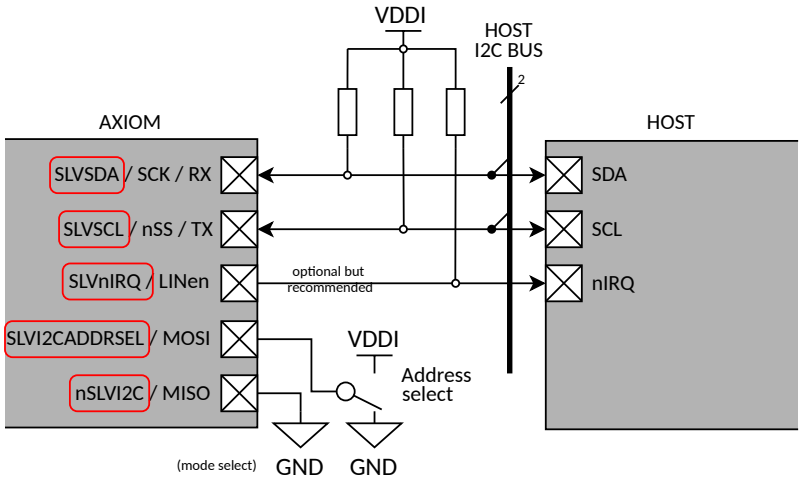


Figure 7.3.2-1: Slave I²C Connections

7.3.3 I²C Protocol

The communications protocol used to access configuration registers in the device and to receive event reports from the device, can be found in **TNxAN00035 aXiom Touch Controller Comms Protocol**. Real-time report collection from the device over the I²C interface has been optimized to work in an interrupt driven mode rather than being polled.

7.4 Slave SPI Mode

7.4.1 Device Selection

In order to communicate with the device the **SLVSCL / nSS / TX** pin must be asserted low for (at least) the duration of the communication. It is OK to permanently connect **SLVSCL / nSS / TX** to GND when in SPI mode, if the AX54A-0D is the only device on the SPI bus.

7.4.2 Connections

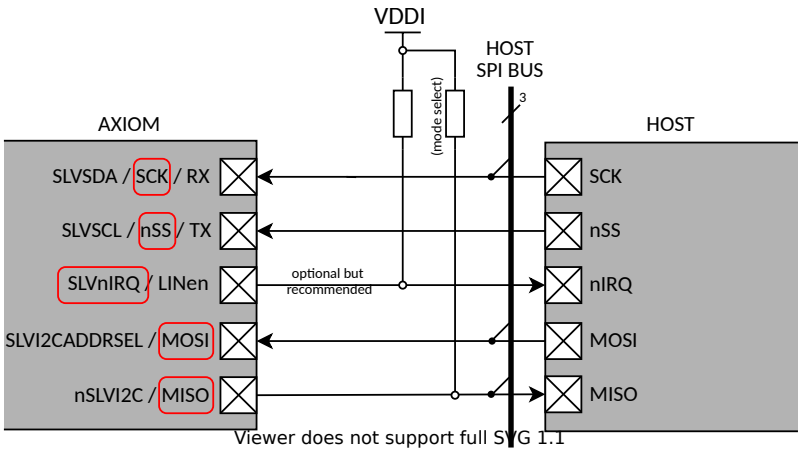


Figure 7.4.2-1: Slave SPI Connections

7.4.3 SPI Protocol

The SPI interface operates in Mode 0[12]. The communications protocol used to access configuration registers in the device and to receive event reports from the device, can be found in **TNxAN00035 aXiom Touch Controller Comms Protocol**. Real-time report collection from the device over the SPI interface has been optimized to work in an interrupt driven mode rather than being polled.

7.5 Slave LIN Mode

7.5.1 Connections

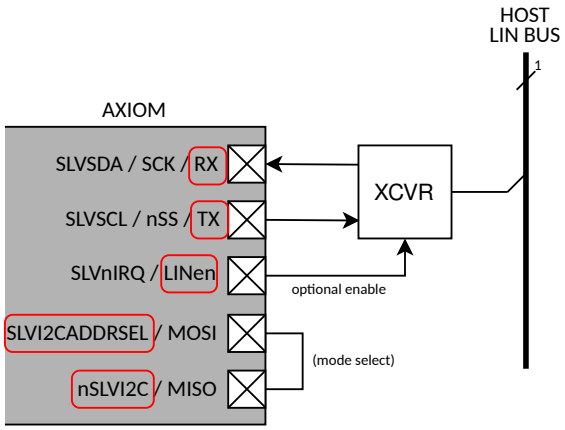


Figure 7.5.1-1: Slave LIN Connections

[12]Clock Polarity:0, Clock Phase:0, Clock Edge:1 (Clock idles at 0, and uses rising edge to sample data, and uses falling edge to shift data).

8 Haptics

In order to provide physical sensation feedback to a user who is pressing on a surface, the AX54A-0D offers a mechanism to trigger a 3rd party Haptic driver device. To qualify when a Haptic effect should be played, the following events can be used to generate the overall trigger:

- Applied force (rising).
- Applied force (falling).

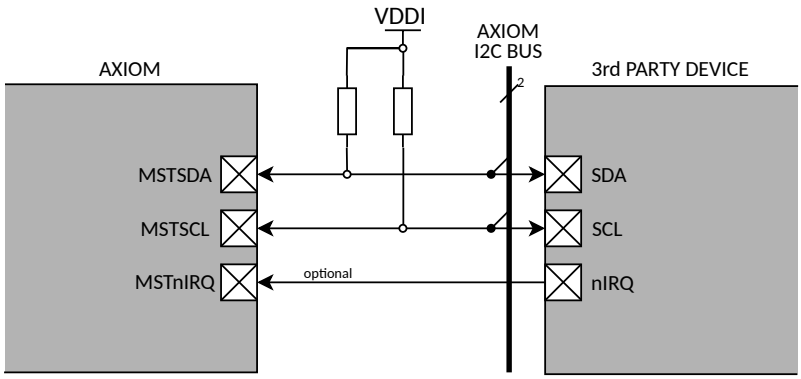


Figure 8-1: Master I2C Connections to 3rd Party Device(s)

aXiom can use the Master Comms port in one of 3 modes to trigger the playback of an effect:

1. In Master GPIO mode; driving a set of 4 output pins to control an actuator. (normally via an amplifier such as an H-Bridge driver).
2. In Master I2C mode[13]; using the Master I2C interface to send commands to trigger a 3rd party actuator device.
3. In Master SPI mode[14]; using the Master SPI interface to send commands to trigger a 3rd party actuator device.

The first method is limited in that it only allows simple effects to be triggered. The second and third methods are much more flexible, as they can transmit a sequence of commands to a device that both define and trigger the effect. A typical example of such a 3rd party actuator device is the Texas Instruments™ DRV2605. This can be connected to the Master Comms port I2C interface of the AX54A-0D and a series of I2C *macro* commands can be defined in the device configuration, to achieve various effects. As part of the I2C sequence, dynamic data can be sent to the device from the AX54A-0D such as force value, effect etc.

For further details see **TNxAN00036 aXiom Touch Controller Haptics Drive**.

[13] Noting that this is not related in any way to the **Host** Interface I2C Mode.
[14] Noting that this is not related in any way to the **Host** Interface SPI Mode.

9 Programming Model

aXiom devices use a register interface called *Touch Controller Protocol*, or TCP, which defines each and every register in the device, how they are organized and accessed. TCP covers configuration and tuning registers, as well as general status and information registers. For the transport of "live" data, TCP also describes a reporting scheme; this is particularly important for host device drivers, because it is the mechanism by which the device sends real-time touch information to the host.

While all aXiom devices use TCP, the exact set of registers and features offered by a specific device do vary. Hence, this general document does not present a detailed programming interface. Instead, you are directed to **TNxAN00087 aXiom AX54A-0D Touch Controller Programmer's Guide**

.

The runtime firmware in aXiom devices is field upgradable using a command and register interface called "Bootloader Protocol" or BLP, details of which can be found in **TNxAN00043 aXiom Touch Controller Bootloader**.

10 Device Characteristics

All quoted ranges are at an operating ambient temperature of 25°C unless otherwise stated.

10.1 Absolute Maximum Ratings

Stresses beyond those listed in Table **10.1-1** may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these, or any other conditions beyond those indicated in **10.2 Operational Ratings** is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Symbol	*Parameter*	*Min*	*Max*	*Units*
VDDA	Analogue supply	-0.3	4	V
VDDI	I/O supply	-0.3	4	V
V_{pc}	Voltage applied to any CMOS pin	-0.5	VDDI+0.5	V
I_{pc}	Maximum source/sink current for any CMOS pin	-25	25	mA
V_{pa}	Voltage applied to any Analogue pin	-0.5	VDDA+0.5	V
I_{pa}	Maximum source/sink current for any Analogue pin	-25	25	mA
T_S	Storage temperature (non operating)	-65	150	°C
T_J	Junction temperature (operating)		125	°C
ESD_{hbm}	ESD rating, human body model[15]		2000	V
ESD_{cdm}	ESD rating, charged device model[15]		750	V

Table 10.1-1: Absolute Maximum Ratings

[15] Discharge direct to device pins. Discharge rating to the sensor/lens in a system is application specific but is typically far higher than this device rating.

10.2 Operational Ratings

10.2.1 Operating Conditions

Symbol	*Parameter*	*Range*	*Units*
T_A	Ambient temperature[16]	-40 to +105	°C
RH_A	Ambient relative humidity (non-condensing)	10 to 90	%RH

Table 10.2.1-1: Operating Conditions

10.2.2 Power Requirements

Symbol	*Parameter*	*Range*[17]	*Units*
VDDA	Analogue supply	2.97 to 3.63	V
VDDI	I/O supply	1.62 to 3.63	V
IDDA	Active analogue supply current (average over frame)	120 to 155	mA
IDDI	I/O supply current (average over frame)	0.005 to 5 (tbc)	mA
N_{VDDA}	Allowable peak-to-peak noise and ripple on analogue supply	85	mV
N_{VDDI}	Allowable peak-to-peak noise and ripple on I/O supply	200	mV

Table 10.2.2-1: Power Requirements

Note that IDDA varies depending on the device's configuration, which defines the measurement types and durations that are performed. For host power supply sizing and thermal calculations, the maximum stated value should be used as an average, with an allowance for +/-25% current variation away from the average during a measurement frame. The chosen regulator must be able to cope with this transient current behaviour.

Also note that IDDI varies significantly depending on the amount of IO activity, but is generally far smaller than IDDA. As noted in **4 Pin Descriptions** VDDA and VDDI are commonly shared and so this current should be added to the overall supply current budget.

10.2.3 Power Sequencing

There are no power sequencing requirements for the application or removal of (or between) VDDA and VDDI. Internal brown-out detection will prevent the device from operating, until both VDDA and VDDC (internal) are properly established. VDDI is not level checked as it does not directly impact the internal operation of the device[18].

CMOS I/O pins should never exceed the limitations stated in Table **10.1-1** (Vpc and Vpa) during power up, operation or power down.

10.2.4 Startup Time

From the rising edge of **nRESET** (or when **VDDA** rises above approx. 2V) to the falling edge of **nIRQ**[19]: < **110ms** typical. At this point the device is fully operational.

10.2.5 Reduced Power Mode

To conserve power during periods of low activity, the device can be configured to enter[20] a Reduced Power Mode (RPM). This trades off first detection latency (from RPM) against power consumption. Typical

[16] Subject to appropriate PCB design.
[17] Treat these values as bounding limits.
[18] ...but clearly VDDI needs to be correctly established in order to communicate with the device.
[19] The first interrupt is created by a "hello" System Manager report to the host.
[20] Either automatically or by command.

power reductions of 2 to 6x are possible, as the RPM measurement rate is reduced. For further details refer to **TNxAN00061 aXiom Touch Controller Reduced Power Mode**.

10.2.6 CMOS I/O Characteristics

Symbol	*Parameter*	*Range*	*Units*
V_{IL}	Logic low input @ 1.8V VDDI	-0.3 to 0.63	V
V_{IH}	Logic high input @ 1.8V VDDI	1.2 to 3.6	V
V_{OL}	Logic low output @ 1.8V VDDI, 1.5mA sink	0.5 max	V
V_{OH}	Logic high output @ 1.8V VDDI, 1.5mA source	1.4 min	V
R_{WPU}	Weak pull up resistance @ 1.8V VDDI (where applicable)	69 - 201	KΩ
I_{IL}	Input leakage current	±1 max	uA

Table 10.2.6-1: CMOS I/O Characteristics (1.8V)

Symbol	*Parameter*	*Range*	*Units*
V_{IL}	Logic low input @ 3.3V VDDI	-0.3 to 0.8	V
V_{IH}	Logic high input @ 3.3V VDDI	2.0 to 3.6	V
V_{OL}	Logic low output @ 3.3V VDDI, 4mA sink	0.5 max	V
V_{OH}	Logic high output @ 3.3V VDDI, 4mA source	2.4 min	V
R_{WPU}	Weak pull up resistance @ 3.3V VDDI (where applicable)	34 - 74	KΩ
I_{IL}	Input leakage current	±1 max	uA

Table 10.2.6-2: CMOS I/O Characteristics (3.3V)

10.2.7 Slave I²C Characteristics

The AX54A-0D implements a Slave I²C interface that is compliant with industry standards. It supports both Standard-mode (100KHz) and Fast-mode (400KHz). Addressing is 7-bit. Clock stretching support by the host *is* required.
Bus timings are as per **UM10204 I²C-bus specification and user manual Rev. 6 — 4 April 2014**. The general form of an I²C transaction is shown below. Additional I/O and timing parameters can be found in the aforementioned document in Table 9 and Table 10.

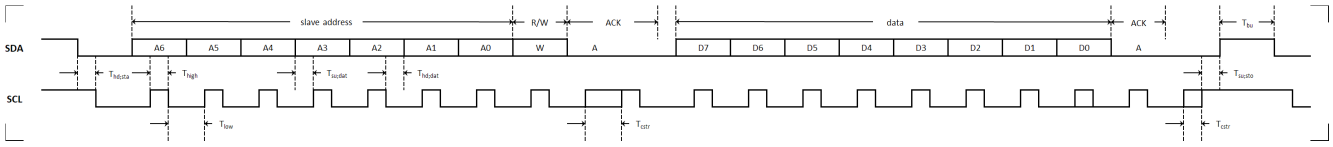


Figure 10.2.7-1: Typical I²C Transaction and Parameters

Symbol	*Parameter*	*Min*	*Max*	*Units*
$T_{hd;sta}$	Start bit hold time	600	-	ns
T_{high}	Clock high period	600	-	ns
T_{low}	Clock low period	1300	-	ns
$T_{su;dat}$	Data setup time	100	-	ns
$T_{hd;dat}$	Data hold time	0	-	ns
T_{cstr}	Maximum clock stretch by slave	-	5	us
$T_{su;sto}$	Stop bit setup time	600	-	ns
T_{bu}	Bus free time between stop and start	1300	-	ns

Table 10.2.7-1: Timings

10.2.8 Slave SPI Characteristics

The AX54A-0D implements a Slave SPI interface that is compliant with industry standards. It supports Mode 0 communication at up to 4MHz. The most significant bits of 8-bit data fields are exchanged first.

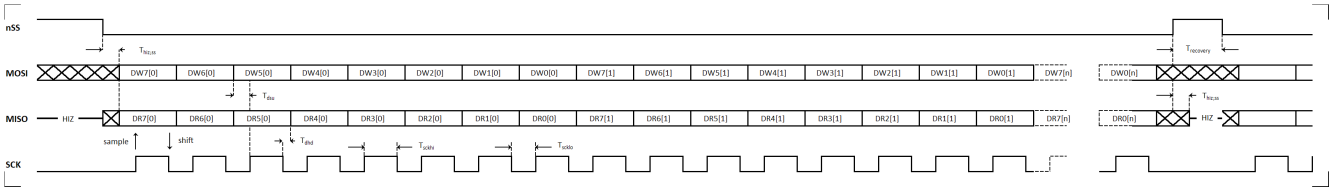


Figure 10.2.8-1: Typical SPI Transaction and Parameters

Symbol	*Parameter*	*Min*	*Max*	*Units*
$T_{hiz;ss}$	nSS transition to MISO transition to/from HiZ	-	20	ns
T_{dsu}	Data setup time (MOSI to SCK)	20	-	ns
T_{dhd}	Data hold time (SCK to MISO)	50	-	ns
T_{sckhi}	SCK high period [21]	100	-	ns
T_{scklo}	SCK low period[22]	100	-	ns
$T_{recovery}$	Slave recovery time, ready for next transfer[23]	-	45	us

Table 10.2.8-1: Timings

[21] Subject to maximum SCK frequency of 4MHz.
[22] Subject to maximum SCK frequency of 4MHz.
[23] The host must ensure that it does not violate this recovery time by ensuring that transfers are spaced apart sufficiently to let the slave prepare for the next transfer. Violating this timing will result in undefined Slave behaviour, possibly lasting beyond the initial violated transfer.

10.2.9 Master I²C Characteristics

The Master I²C interface implemented in the AX54A-0D is intended for communication with one or more 3rd party slave devices. The characteristics of the interface are identical to those of the Slave I²C interface. See **10.2.7 Slave I²C Characteristics** for details. The Master I²C interface supports clock stretching by a connected slave.

10.2.10 Capacitance Ranges, Thermistors and Drive Limits

Symbol	Parameter	Absolute min	Recommended min	Recommended max	Absolute max	Units
F_{EXC}	Excitation frequency	50	100	500	1000	KHz
$V_{EXC-ABS}$	Abs cap excitation voltage pk-to-pk (centered around VDDA/2)	-	2.4	2.4	VDDA-0.9	V
C_{SHIELD}	Total capacitance to GND on SHIELD	-	-	-	20	nF
$C_{CTS-ABS}$	Total Abs Capacitance to GND on any CTS pin	-	-	-	1000	pF
$C_{CDS-ABS}$	Total Abs Capacitance to GND on any CDS pin	-	-	-	1000	pF

Table 10.2.10-1: Capacitance Ranges and Drive Limits

Note that F_{EXC}, $V_{EXC-ABS}$ can be directly controlled via the device's configuration registers, so ensuring that the limits are met by tuning. The capacitance limits relate to external factors arising from the attached sensor and associated tracking.

Symbol	Parameter	Value	Tolerance	Dielectric/Type	Units
$C_{CALCAP0}$	CALCAP reference capacitor 0	200	1%	NP0 / C0G	pF
$C_{CALCAP1}$	CALCAP reference capacitor 1	100	1%	NP0 / C0G	pF
R_{THERM0}	THERMISTOR0 resistance	10	5%	NTC B≈4250K	KΩ
R_{THERM1}	THERMISTOR1 resistance	10	5%	NTC B≈4250K	KΩ
R_{REFRES}	REFRES resistance	10	1%	any	KΩ

Table 10.2.10-2: CALCAP and THERMISTOR Requirements

10.2.11 Non-volatile Memory Characteristics

Symbol	*Parameter*	*Range*	*Units*
N_{EC}	Number of erase cycles	10000	cycles
t_{DR}	Data retention @ 85°C T_A	10	years
EDAC	Error detection and correction	Detect and correct all 1-bit errors Detect all 2-bit errors	-

Table 10.2.11-1: Non-volatile Memory Characteristics

10.2.12 Device BIST Capabilities

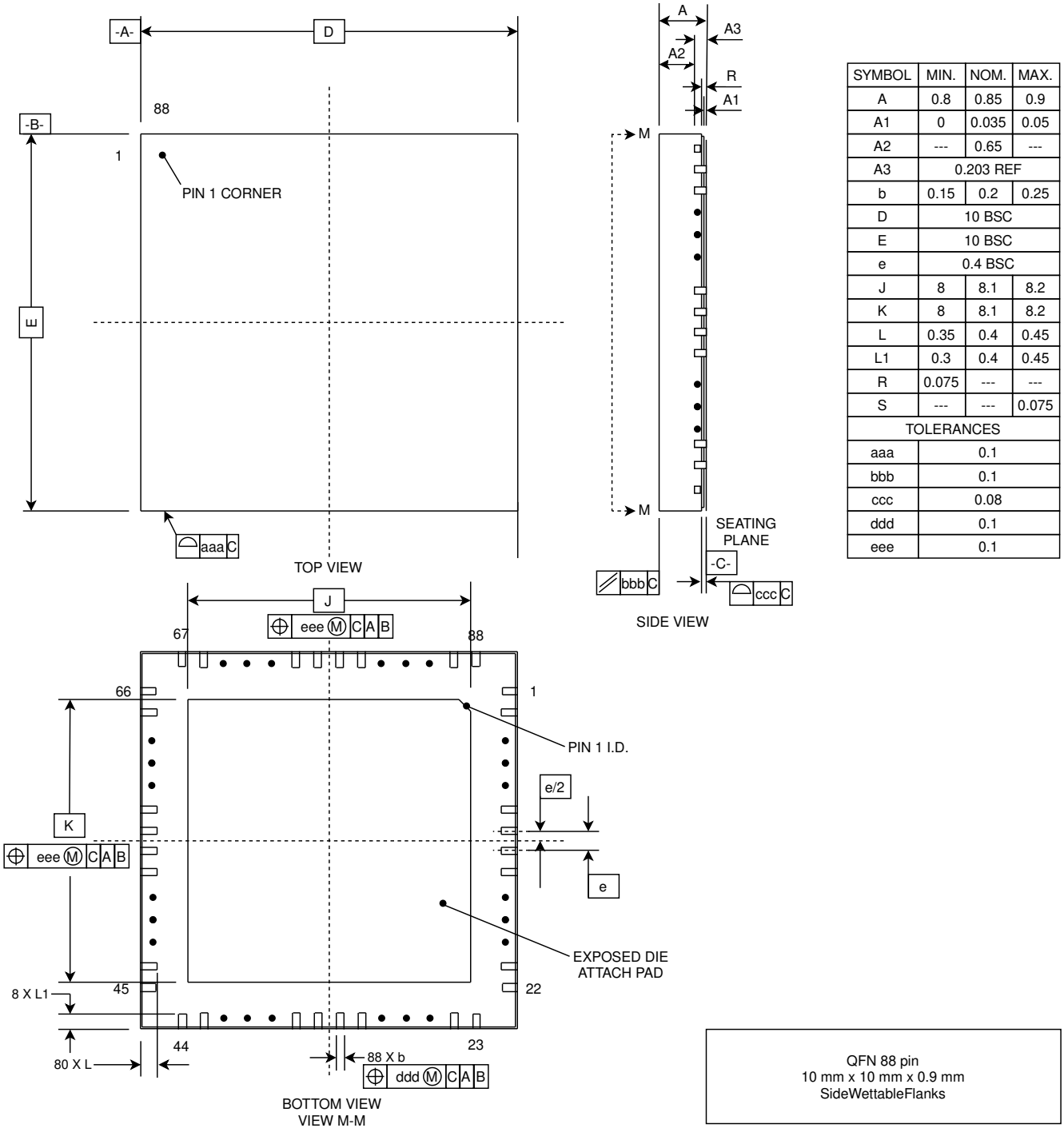
- RAM self tests.
- NVM EDAC (see **10.2.11 Non-volatile Memory Characteristics**).
- Code execution protection using Watchdog Timer clocked by separate internal oscillator.
- Checksum over NVM.
- Checksum over volatile configuration.
- Checksum over non-volatile configuration.
- Out of range VDDA detection.
- Out of range Acquistion Engine reference capacitor checks.
- Interrupt pin test.
- Cross-check main CPU and RTC/watchdog oscillators against each other.
- Configurable "Heartbeat" report to host allows BIST trigger (limited range) and live status plus, a cross check of the timing period/CPU main oscillator rate.

10.2.13 Sensor BIST Capabilities

- All CTS sense channels allow detection of impedance leakage of up to 200K■ to any net.
  - Test can be triggered by host command and optionally run at device boot-up.
- All CDS sense channels allow detection of impedance leakage of up to 200K■ to any net.
  - Test can be triggered by host command and optionally run at device boot-up.
- Detection of opens on CTS electrode channel by configurable signal limits.
  - Test can be triggered by host command and also run periodically using Heartbeat tick.
- Detection of opens on CDS electrode channel by configurable signal limits.
  - Test can be triggered by host command and also run periodically using Heartbeat tick.
- VGE pre-load indication using CALCAPs as reference for CDS channels allows factory go-no-go on assembly tolerance.

Appendix A Package Drawings

A.1 QFN88-10100904



SYMBOL	MIN.	NOM.	MAX.
A	0.8	0.85	0.9
A1	0	0.035	0.05
A2	---	0.65	---
A3	0.203 REF		
b	0.15	0.2	0.25
D	10 BSC		
E	10 BSC		
e	0.4 BSC		
J	8	8.1	8.2
K	8	8.1	8.2
L	0.35	0.4	0.45
L1	0.3	0.4	0.45
R	0.075	---	---
S	---	---	0.075
TOLERANCES			
aaa	0.1		
bbb	0.1		
ccc	0.08		
ddd	0.1		
eee	0.1		

QFN 88 pin
10 mm x 10 mm x 0.9 mm
SideWettableFlanks

Figure A.1-1: QFN88 10x10x0.9x0.4 Package Drawing

A.1.1 Layout and Routing Considerations for VDDA tracks

To maximize SNR performance special care must be taken when laying out VDDA power traces.

The maximum tolerated voltage drop *between* VDDA pins varies. The table below should be used for estimation of device current consumption into each VDDA pin to allow estimation of the voltage drops in your PCB layout (the IR voltage drop). You must then check that they are within the allowed range as listed below.

Pin	Type	Max Current (mA)	ΔV
23	VDDA	30	<2mV ΔV between these pins
88	VDDA	30	
40	VDDA	5	<5mV ΔV from other VDDA power pins
64	VDDA	100	<5mV ΔV from other VDDA power pins

The images provided are for general guidance. Gerber files for reference designs can be provided by TouchNetix on demand.

Please note: any reference material provided shall be taken as guidance only. PCB designers must ensure to run power/current analysis on their designs to make sure they are compliant with the requirements outlined above.

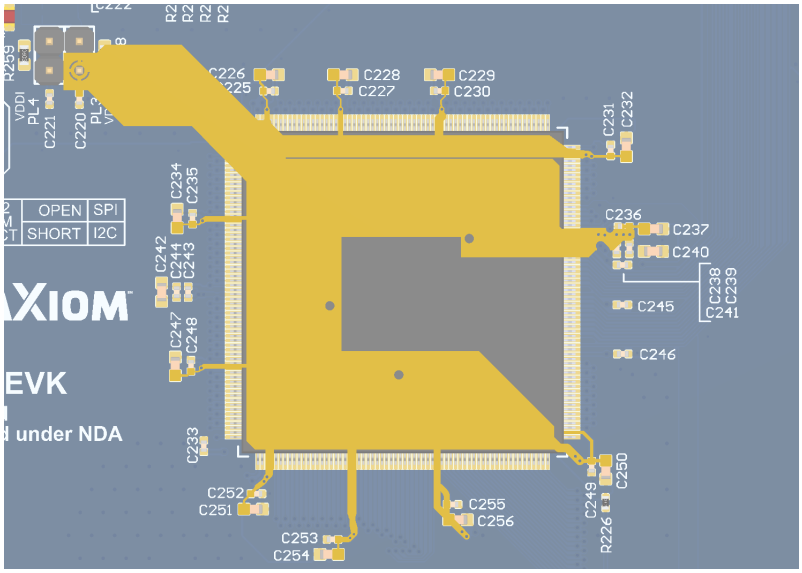


Figure A.1.1-1: C-shaped power routing, balanced amongst all VDDA pins. Using AX198A as reference, guidance can be applied to this device.

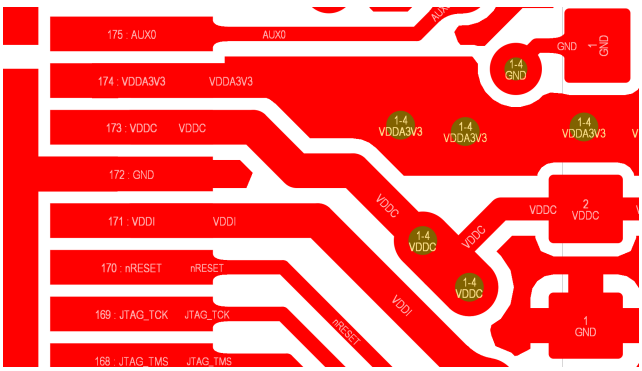


Figure A.1.1-2: Note the use of the widest possible tracking and multiple vias for all VDD tracks. Using AX198A as reference, guidance can be applied to this device.

Appendix B References

TNxAN00035 aXiom Touch Controller Comms Protocol.
TNxAN00037 aXiom Touch Controller Sensor Channel Routing.
TNxAN00043 aXiom Touch Controller Bootloader.
TNxAN00045 aXiom Touch Controller Comms Quick Start Guide.
TNxAN00047 aXiom Touch Controller Sensor Testing.
TNxAN00048 aXiom Touch Controller EMC Report.
TNxAN00051 aXiom Driver Guide.
TNxAN00052 aXiom Project Flow.
TNxAN00056 aXiom Self Test.
TNxAN00061 aXiom Touch Controller Reduced Power Mode.

TNxAN00087 aXiom AX54A-0D Touch Controller Programmer's Guide.
TNxAN00088 aXiom TactoSense Design Guide.

Note: Release of the above documents may require a specific NDA to be in place, please contact TouchNetix for more details.

Appendix C Legal Copyright and Disclaimer

Appendix D Document History

Revision	Date	Change summary
A1	23/01/2024	Preliminary release with SHIELD pin change
A2	12/03/2024	Correct pins 71 and 72 on device pin map